ACTS

ATARI COMPUTER TEST SYSTEM

ATARI PRODUCT ENGINEERING

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I. INTRODUCTION

The Atari Computer Test System (ACTS) was developed to test the Atari Home Computer System (400/800). It rigorously tests the product for a long period of time (known as Burn Time). Excercising Ram, Rom, display (ANTIC, GTIA), PIA (Peripheral Interface Adapter), POKEY (Pot, Keyboard Interface) Microprocessor, and the Power Supply.

The system is comprised of Several computers linked by a communications network. The individual product is excerised by the SLAVE unit (a Motorola 6800 based micro-computer) via a custom interface device known as the Test Head. Each SLAVE is capable of handling 128 Test Heads (this arangement is called a 'BAY'). The SLAVE is controlled by the Line Concentrator (a Data General S130,S140), also known as LC, which controls the actual test sequence and determins an interim pass or fail status.

Tests are issued to the SLAVE which inturn passes them to the Unit Under Test (UUT) and executes any other functions specific to that test. A pass or fail is sent back to the SLAVE who then asks for a detailed error report which is 'shiped' to the LC. The data gathered by the LC is then shipped to MOTHER (a Data General C350,MV8000). MOTHER uses the data to generate graphs, analysis' and other useful information for Manufacturing. These graphs and analysis' are used for determining the general status of the product.

Mother also can give a trouble shooter useful information about the failure mode of the product under investigation. She looks for like occurances of the same failure and shows some possible 'fixes' for same. This function is known as the Heuristic Data Base. Heuristic meaning self learning. The more MOTHER is taught the better judgment she can make on a given faiulre.

II. Basic Description

The Home Computer Product, also known as Unit Under Test (UUT) is tested on a rack with 127 other UUT's. The SLAVE is told to apply power to the UUT and check power supplies (+5 volt, +12 volt, ground and current) parametrically to see if the values are within specification. Then a check is made to see if the UUT can 'talk' (communication is acheived over the four player ports via the PIA). If all goes well at this point, The UUT is somewhat functional.

If the UUT made it this far a thourough check is made of the PIA. This is done by sending data back and forth between the slave and UUT and verifying that the data received is the same as the data sent. Next, a basic test of the Ram is executed (locations 0-512 are checked - operating ram and Stack). If the UUT survives these preliminary tests, a long intensive test commences.

III. TEST SEQUENCE DESCRIPTION

First, the Ram is put through a more extensive test. Depending on the ram size (8, 16, or 32 K (1024)) locations are tested. In step 1, the data lines are checked (a bit is 'walked' through the data bus looking for shorts and opens), and the address lines are checked (a bit is 'walked' through the address bus looking for shorts and opens). In step 2, a data pattern is 'written' through out memory and checked to see if it arrived there intact. The Stack (locations 256-511) is then checksummed (all data is added togther), The UUT then pauses for 1 second, after which the Stack is re-checksummed. The two checksums are compared to see if they are the same. If the compare fails, Refresh (the ram must be 're-charched' to maintain its data) has a problem. The rest of the ram (locations 512 to ram size) are also checked for refresh failure by verifying the original pattern (written in step 2). Any errors detected are sent to the SLAVE.

Second, the Operating Sytstem, contained in the three Roms (read only memory), is checksummed and verified against a preset value.

Third, The POKEY's serial port is checked to see if it can send and receive characters. This is done interactively between the SLAVE and UUT. All modes of the POKEY are tested, asyncronous (the SLAVE and UUT use their own clocks) and syncronously (data is transmitted using the SLAVEs clock and the using the UUT's clock). This is done by sending characters to and from the SLAVE to the UUT and then verifying that the characters received were the same as the ones sent.

Fourth, the control lines of the PIA are tested. This is also done interactively between the SLAVE and UUT. Three of the lines are first brought high (5 volts) and then each is brought low (0 volts). Shorts and opens are found and reported to the SLAVE. Then a parametric test is done on the motor control line (used for controlling the 410 Program Recorder) to see if the voltages are within specification.

Fifth, the interrupt control lines (the microprocessor can be temporarily interrupted on command) generated from the PIA and POKEY are tested. This can be very dangerous because the processor first must go to the operating System rom before the test cartridge. If there is something wrong with the Rom, the UUT may never communicate with the SLAVE again. This usaully results in a 'time-out' error.

Sixth, the Light Pen port of the ANTIC is exercised. There are two registers in the ANTIC that show the position of the light pen. The Light Pen port is activated by the SLAVE. If the Light Pen port operates the UUT will see a certain value in the ANTIC registers. This value is checked against a known correct value. If it is found to be incorrect, the UUT sends an error to the SLAVE.

Seventh, The eight (8) POT ports are tested. The SLAVE sends a 5 volt signal to each of the ports. The POKEY has a register for each pot that represents the voltage applied to that port. This value is sent to the SLAVE which checks it against a known window (a low limit and a high limit). If the value does not fall within this window an error is indicated.

Eight, the trigger lines of the GTIA are tested. The SLAVE toggles (takes low then high) the four triggers one at a time. The UUT checks to see if the trigger ports indicate whether or not they did toggle. The UUT also checks to see if their was any interraction, caused by shorts between the lines. The UUT then reports any errors to the SLAVE.

lastly, a soft reset (The UUT is told to go back to start at the beginning) takes place. This is done because the initial check (power, initial communications) will take place again.

At this point the Line concentrator checks to see if a max error count has been reached or if no errors were found if the 40 hour burn time is complete. If neither of these conditions exist, the entire test sequence is repeated. If these conditions do exist, approriate data is shipped to MOTHER and stored in a data base for easy access.

IV. PRODUCTS TESTED

The ACTS system is capable of testing any product that ATARI manufactures. current products being tested are, 400/800 (computer console), 850 (interface module), 810 (disk drive), 830 (modem). The system was also modified to test the Video computer system (VCS). however, it is not being used to test VCS at this time.

The test sequence for each product is somewhat different, but the general test philosophy is the same.

Some product is tested at board level as well. Each of the boards that go into a 400 or 800 is are tested on board level stations (a board level station is comprised of two Test Heads connected to a single SLAVE). The 850 mother board is also tested at board level.